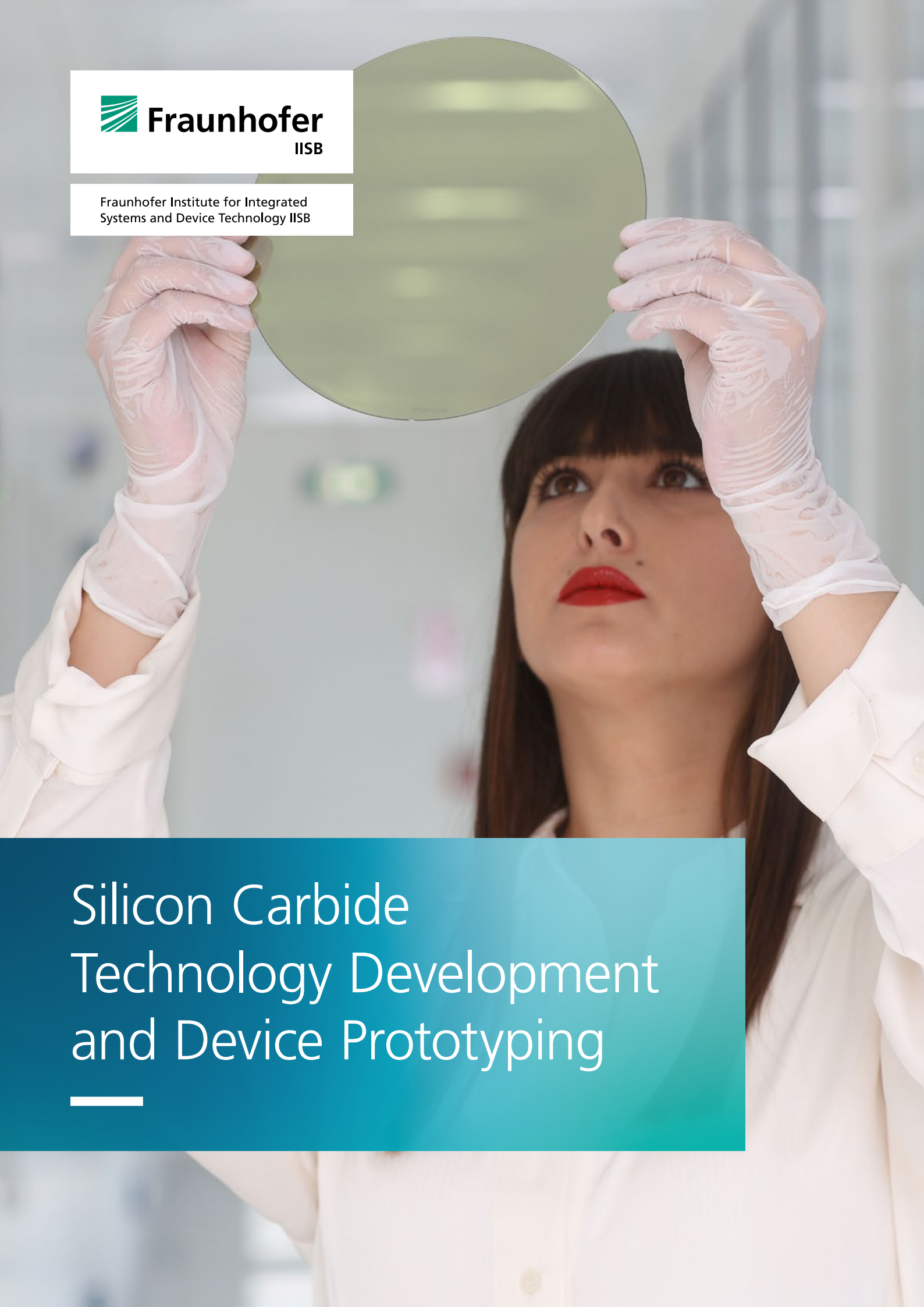

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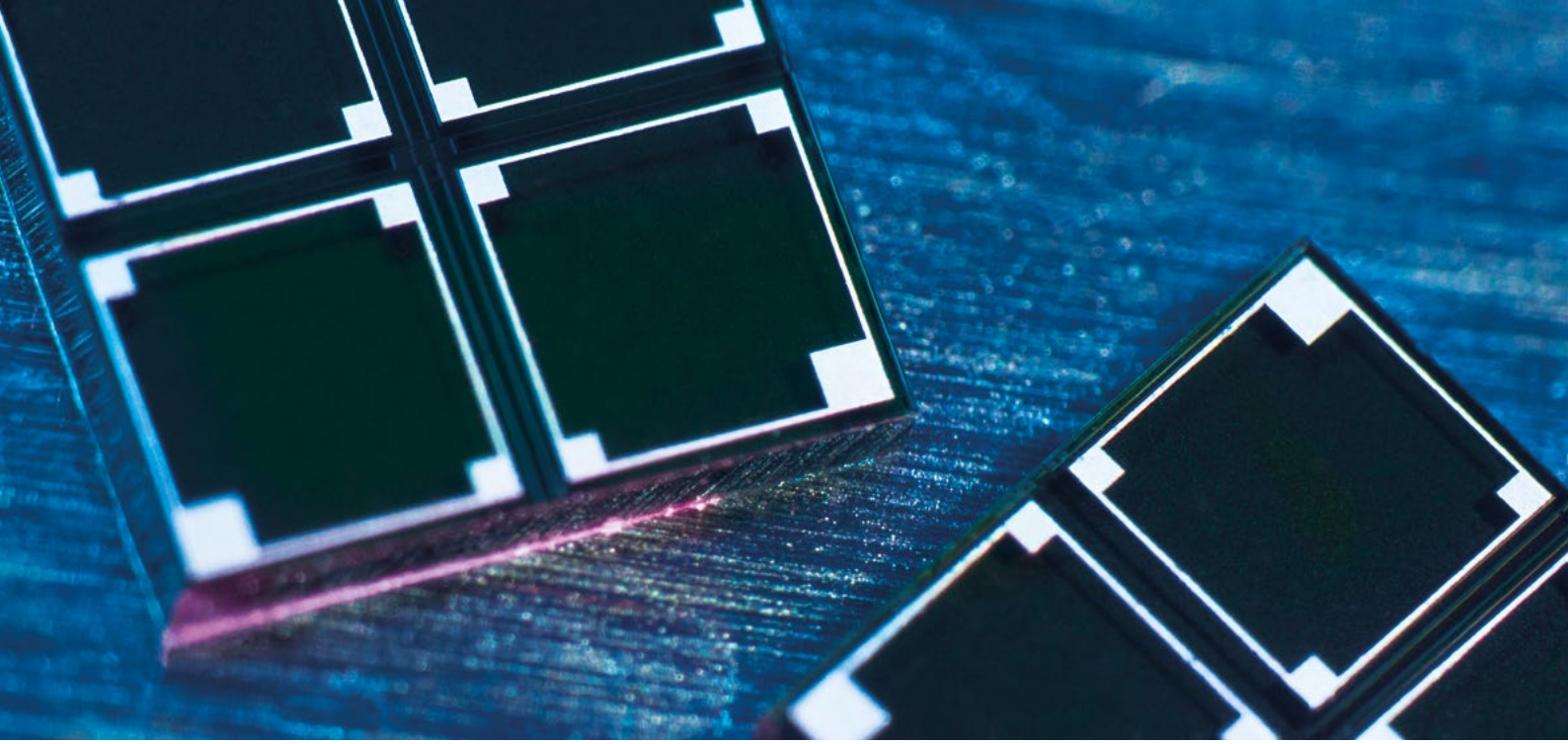
Silicon Carbide Technology Development and Device Prototyping



2 x 2 UV diode sensor array

Customized Solutions in SiC

The Fraunhofer Institute for Integrated Systems and Device Technology IISB conducts applied research and development in the fields of Power Electronics, Materials for Electronics, Electric Mobility and Energy Electronics.

Drawing on twenty years of ongoing cooperation with partners from SiC industry and research, Fraunhofer IISB has been established as Germany's hotspot for silicon carbide power device manufacturing on a 150 mm SiC line.

4H-SiC is the ideal semiconductor for the realization of high-voltage and high-power electronic devices due to its outstanding material properties.

Our mission is to share our long standing experience with the customers and to provide them with distinct SiC power device prototypes for newly arising markets.

π-Fab®

π-Fab: Electron Device Prototype Fabrication

Based on more than three decades of experience in silicon microelectronics research and development, IISB has extended its activities to industry-oriented low-volume prototype fabrication of custom-tailored electron devices on Si and SiC.

The ISO certified prototyping services are offered and performed under the brand name π-Fab. Furthermore, π-Fab supports its customers with particular processing steps as well as whole process modules, including lithography, oxidation, LPCVD, ion implantation, annealing, dry and wet etching, metallization, diffusion, layer deposition, metrology, passivation, wafer thinning, laser anneal, PECVD and ALD, and others.

The modular construction allows for the integration and extraction of partially processed wafers at any given point within the process

Panoramic view of the processing line for silicon carbide at Fraunhofer IISB

chain. Additionally, quality management and statistical process control form the frame in order to meet our customers' individual requirements.

Furthermore, π-Fab is designed as a platform where equipment assessment and optimization, or manufacturing control issues for customers can be covered.

Flexibility as a matter of principle

The unique characteristic of π-Fab is a high flexibility in wafer material and size. Silicon wafers with diameters of 150 mm and 200 mm are handled by default, further diameters on request. The process line is based on a 0.8 µm Si-CMOS technology. To keep the flexibility high, an advanced contamination control is available.

Moreover, special attention is turned to silicon carbide (SiC) device processing on 150 mm and 200 mm wafers. To realize all specific SiC process steps, such as epitaxy, ICP dry trench etching, growth of silicon dioxide, implantation at elevated temperatures, implant activation annealing, or ohmic contact alloying, additional equipment is provided in π-Fab.

The principle of flexibility is also exemplary for our additional activities in nanostructuring and inorganic thin-film electronics.

For this purpose, particular equipment, like nano-imprint and advanced FIB-preparation or glove boxes and extended sputtering tools, is available.

Core Competencies

- Simulation and modeling
- Homoepitaxy and defect engineering
- Device and circuit design
- Full power device manufacturing
- Wafer thinning and packaging
- Device characterization

SiC Power Device Prototypes

- Diodes (SBD, PIN, MPS)
- MOSFETs (planar, trench)
- Specific devices (bipolar, CMOS, sensor)
- Industry collaboration towards qualified high-volume foundries

Markets

- Battery electric vehicles (BEV) and electric vehicles (EV)
- Renewable energies (wind, solar)
- Power grid

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Additional Information

SiC Services:
iisb.fraunhofer.de/sic

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SiC VDMOS Technology with Self-Aligned Channel

Processed 150mm 4H-SiC wafer with 1.2 kV VDMOS transistors

SiC Power MOSFETs combine the features of nearly ideal switching with superior electrical and thermal properties of wide-bandgap semiconductor materials. High breakdown voltage of the vertical device is supported on a high-quality epitaxial layer, while threshold voltage and electrical current transport are precisely defined by ion implantation. Top and bottom sides of the devices are metallized for assembly in power modules

The on-state resistance for power MOSFETs is still dominated by the channel resistance, especially for voltage classes below 3 kV. Therefore, an optimized channel design is of high importance for a high-performance device. Technological limitations, like overlay accuracy of the lithography, can lead to a reduction of blocking voltage due to short channel effects for edge-of-technology channel design. To reduce the influence of technological parameters for high yield at small channel length, a self-aligned channel process has been introduced.

After the first implantations, a thick Polysilicon layer is deposited on the scattering oxide. The hard mask is structured by dry etching, with etch stop on the oxide. This hard mask serves as an ion-stop for the PWELL Aluminum implantation. Subsequently, a nitride layer is deposited. The layer thickness of this layer defines the channel length. By anisotropic dry etching of this layer, a spacer is formed. The NPLUS (Source) implantation is performed with the now modified hard mask.

Advantages

- Typical $R_{DS(on)}$ below 7 mΩ·cm² for 1.2 kV
- Homogeneous channel length over the wafer
- Independent of lithography misalignment
- Channel length can be controlled by processing parameters (Nitride film thickness)
- High temperature implantation with self-aligned channel hard mask

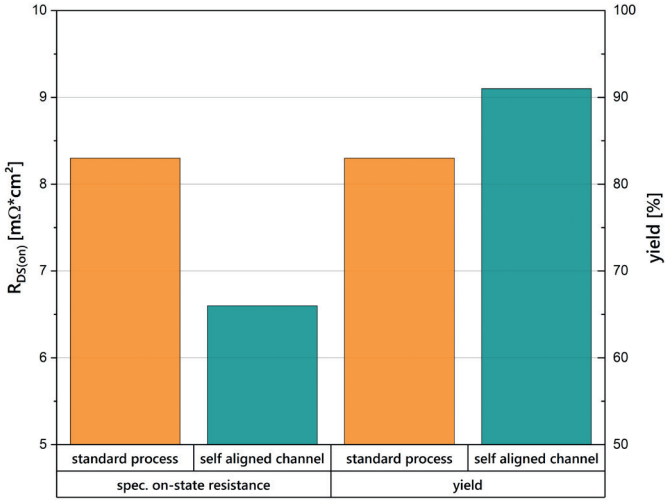

Fig. 1: On-state resistance ($R_{DS(on)}$) and yield values for power MOSFET devices processed with standard lithography process (channel 1 µm) and self-aligned channel process (channel 0.6 µm)

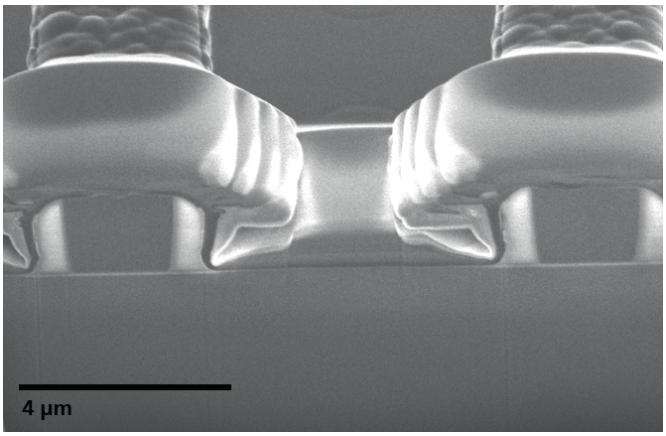

Fig. 2: FIB-cross section of self-aligned channel hard mask after structuring of nitride Spacer

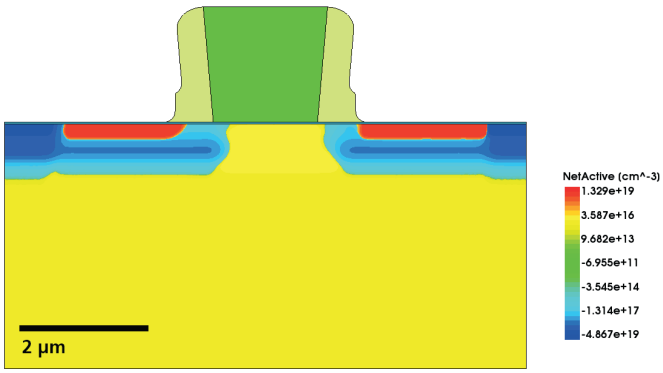

Fig. 3: Process simulation results for self-aligned channel process (hard mask structuring)

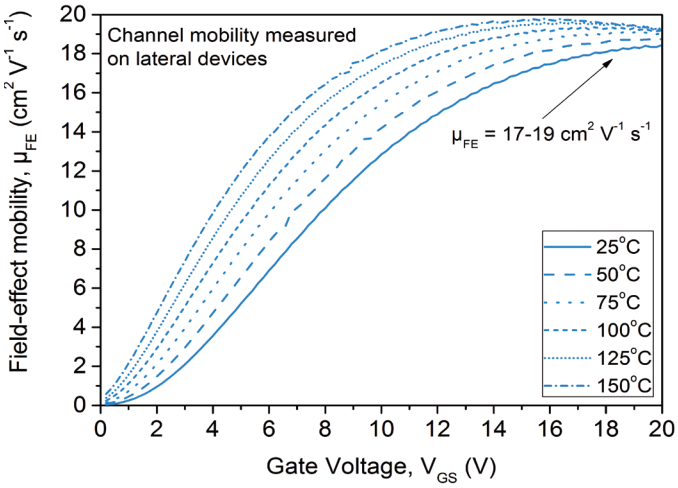

Fig. 4: Example of process technology optimization: Oxide and semiconductor/oxide interface optimized for channel mobility and lifetime

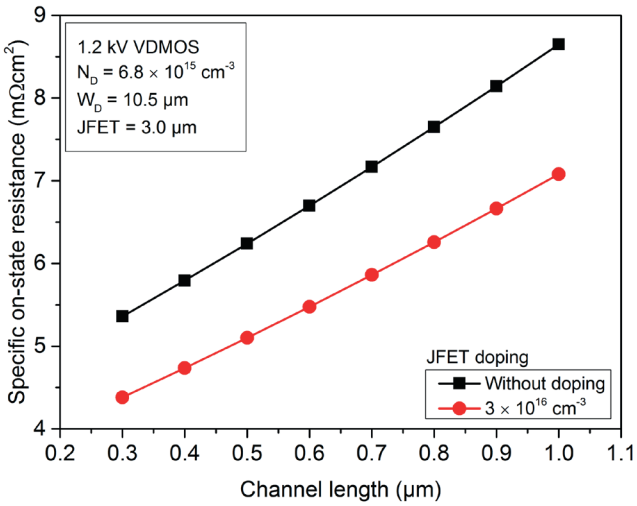

Fig. 5: Specific on-state resistance in dependence of channel length for power MOSFET with and without JFET implantation

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1200 V SiC Trench MOSFET

1200 V SiC TrenchMOS devices on 150 mm 4H-SiC wafer

One approach to further increase the integration density of a Power MOSFET is to introduce a vertical instead of a horizontal channel. The device patterning is realized via trench plasma etching. The reduced cell-pitch of the so-called TrenchMOS due to the absence of a JFET region allows to minimize the chip area and ultimately save chip costs. In addition, the increased channel mobility on the trench sidewall leads to an overall on-resistance ($R_{DS,on}$) reduction compared to Planar MOSFET technology. However, as device architectures becomes more complex, additional manufacturing risks arise. In principle, the n^+-source and p-well regions are implanted in the entire active area. Subsequently, trench structures are formed into this implanted area. Whereas maximal alignment accuracy can be obtained, a drawback of trench-last process is the difficulty to control the etching behavior of the implanted 4H-SiC, which is strongly dependent on the doping concentration. Therefore, the manufacturing process, in which a formation of trenches is followed by implantation (trench-first process), was proposed to form curved trench geometry by a reshape process for reducing high dielectric field concentration at trench bottom corners. Moreover, it is crucial to achieve a high resolution and precise alignment for a mask-compliant structure, which comes with significant lithography system related limitations that impose further high costs. To overcome these challenges, a self-aligned manufacturing process for the formation of the n^+-source and p-well areas, whose alignment is essential for device functionality, was developed at the IISB.

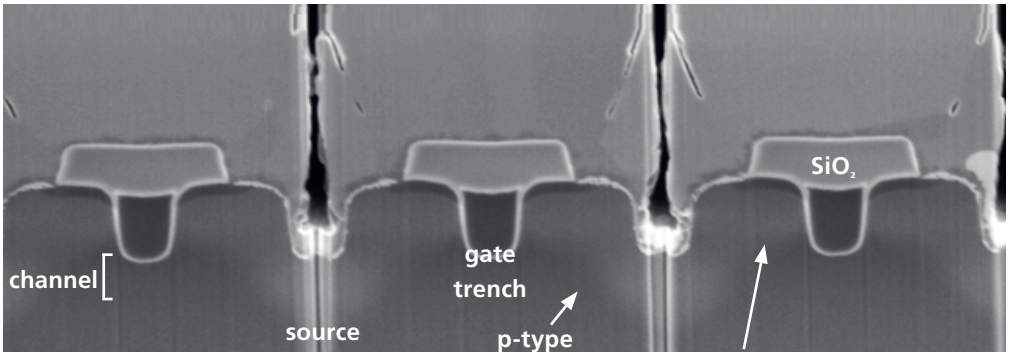

Fig. 1: SEM cross-section image of fabricated SiC TrenchMOS using proprietary trench first technology [1]

[1] Patent pending

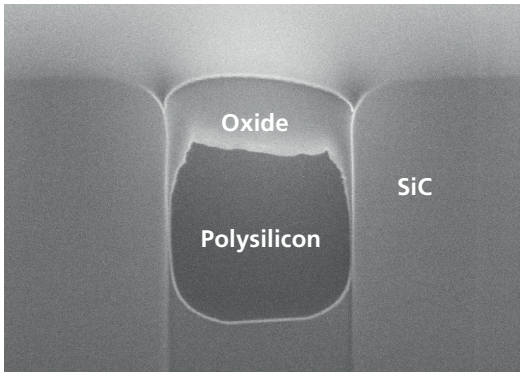

Fig. 2: SEM cross-section image of trench profile prepared via FIB after oxidizing the planarized polysilicon

By oxidizing the previously deposited and planarized polysilicon in the trenches, as depicted in Fig. 2, a self-aligned implantation mask for n^+-source and p-well region is formed that is estimated in advance via process simulator modeling the actual trench shape and oxidized polysilicon. This eliminates the risk of device failure due to misalignment of the corresponding lithography layers. With that, the major benefit here is that implantation for n^+-source and p-well regions within the active area is independent on restrictions regarding the resolution limit and alignment accuracy of the photolithography system. Therefore, the use of a self-aligned process compensates the increased technological effort for TrenchMOS production and simplifies the manufacturing process. Consequently, the production yield increases by minimizing the risk of misalignment of the n^+-source and p-well regions within the active area.

Fig. 3 shows static electrical characteristics in the on- and off-state of the fabricated device shown in Fig. 1, compared with profiles from numerical model and the device simulation. The $R_{DS,on}$ is obtained between 3 and 4 mΩcm² and the device is normally off between 4 and 6 V that can be further improved by design and gate oxide optimization for higher mobility, dielectric breakdown field strength and improved threshold voltage shift. The blocking capability is accomplished up to the target value 1.2 kV that has room for improvement, e.g., a higher shielding effect.

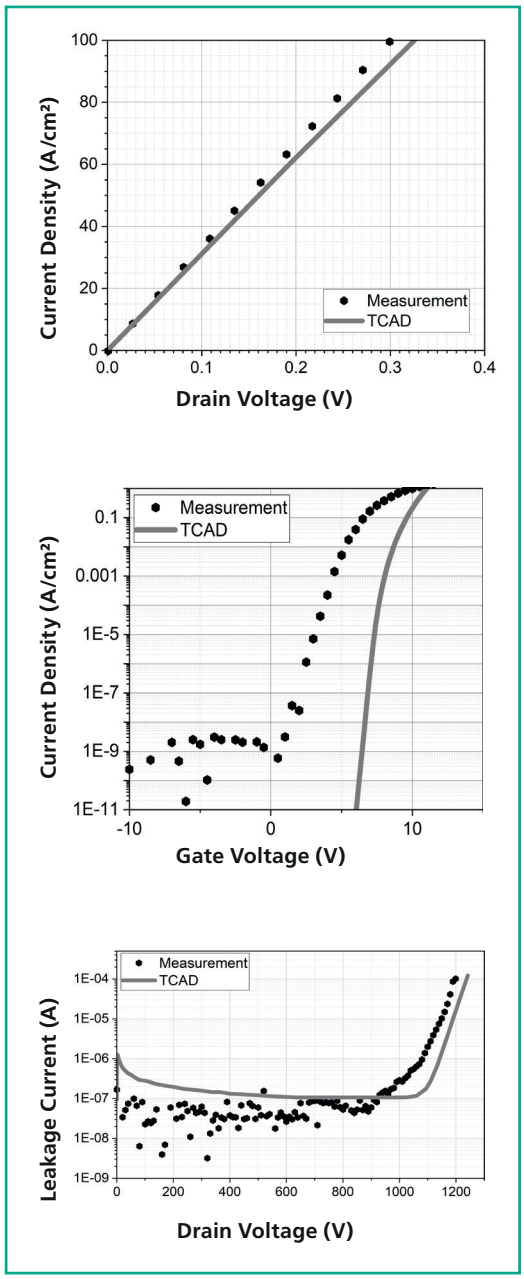

Fig. 3: Output characteristic (top), transfer characteristic (middle) and blocking characteristic (bottom)

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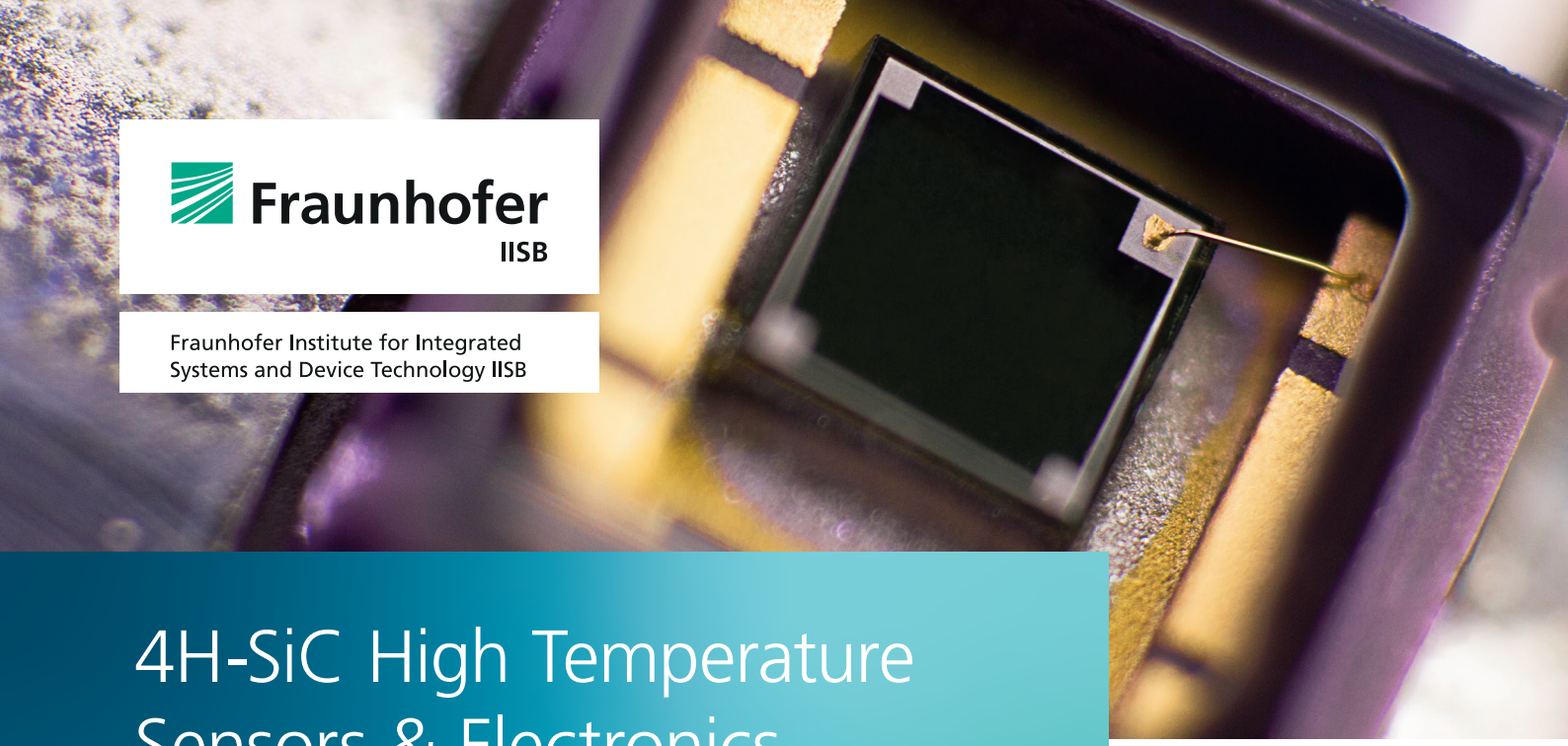

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4H-SiC High Temperature Sensors & Electronics

CMOS Technology Based Sensing and Signal Processing Operable up to 600 °C

Mounted 4H-SiC UV sensor

General Description

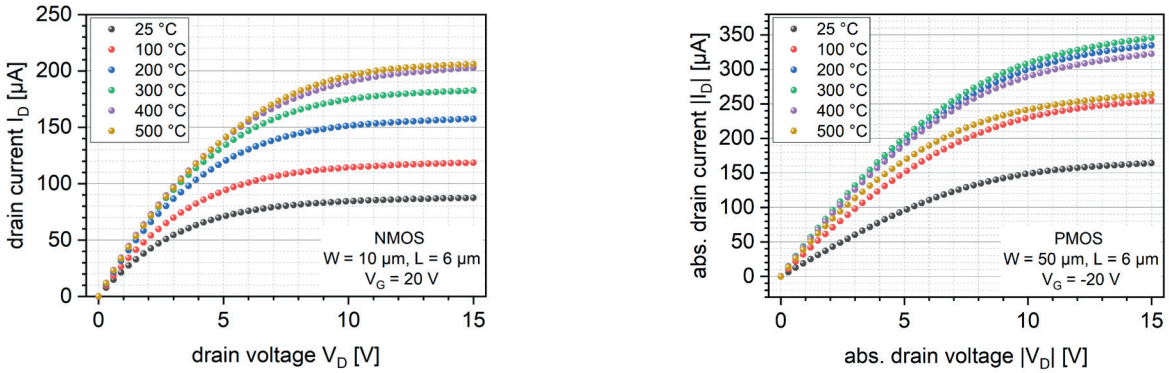
- Mixed-signal circuits operating in harsh environments, including temperatures up to 600 °C
- Combination of sensing function – such as temperature, UV, and magnetic fields – with on-chip amplification and high voltage Smart Power option in an accessible CMOS technology

EUROPRACTICE IC Service*

- Technology also available as multi-project wafer offer through EUROPRACTICE, including custom solution support
- Design kit with simulation models available

Advantages and benefits

- Operable at significantly higher temperatures compared to Si
- Resistant against harsh environmental conditions
- Compact single chip solution due to monolithic integration, replacing external amplifier and reducing sensor signal loss
- Custom electrical characterization available
- Prototype packaging options available upon request
- Cost reduction due to monolithic integration
- Lower entry budget by multi-project wafer option as well as independent dedicated fabrication or R&D runs possible
- Increased market volume through multisensor solutions



Output characteristics of a 4H-SiC NMOS 10/6 (left) and PMOS 50/6 (right) at specific temperatures

Multi-sensor Platform Capability

Temperature

- Temperature-sensitive diode operation under constant current forward bias mode:
  - High sensitivity up to 4.5 mV/K
  - High linearity up to 500 °C
  - Best-in-class high temperature performance of semiconductor-based sensors
- PTAT circuit sensitivity:
  - Typically 0.2 mV/K
  - Tunable by input current ratio
  - Unaffected by the temperature dependence of the integrated circuit

UV Radiation

- Tunable responsivity
- Maximum at 260 nm: 110 mA/W
- Nearly constant responsivity between 270 nm and 300 nm
- Typical maximum external quantum efficiency of 55 %

Magnetic Fields

- Magnetic field FET
- Split drain MAGFET
- Vertical Hall (cross) bar devices
- Suppressed sidewall magnetic injection magneto-transistor

Towards Smart Power Technology

- On-chip combination of low power and high power devices such as high voltage VDMOS or RESURF LDMOS devices
- High-side capability by well isolation

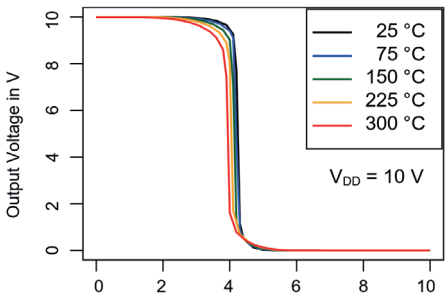
Mixed-Signal ICs

Core Devices

- CMOS technology consisting of NMOS, PMOS and resistors
- Silicon-like channel mobility ratio
  - $\mu_{NMOS} / \mu_{PMOS} = 2.6$ @ 300 °C
  - $\mu_{NMOS} / \mu_{PMOS} = 3.9$ @ 500 °C

Analog and Digital Electronic Circuits

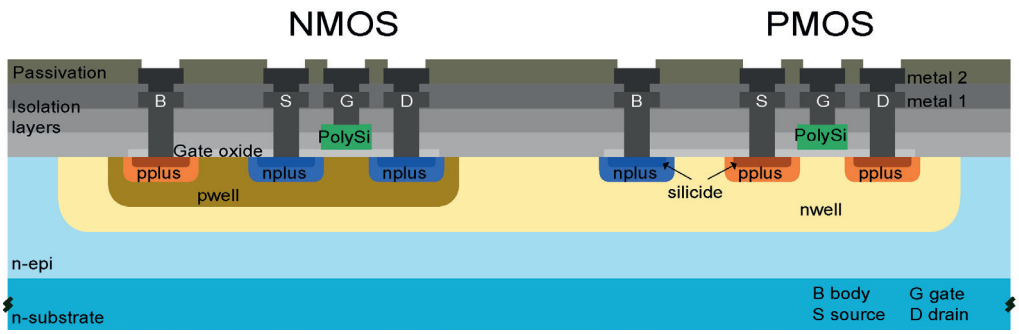
- Differential amplifiers and oscillators
- Comparators
- Current mirrors
- Output buffers
- Inverters and flip-flops
- State-machines and memory



Transfer characteristic of a 4H-SiC CMOS inverter at specific temperatures

Signal Conditioning and Processing

- Analogue to digital converter
- Pre-amplifier
- Transimpedance amplifier



Schematic illustration of the IISB CMOS technology

Additional Information

***EUROPRACTICE IC Service:**
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Monolithically Integrated SiC Circuit Breaker

Self-Supplied, Self-Sensed and Self-Sustained up to 900 V_{DC}

150mm »SiC DC-Breaker« wafer fabricated at Fraunhofer IISB

For high power DC applications, the development of solid state circuit breakers (SSCB) is necessary and has seen a variety of different approaches. The proposed prototypes represent the first monolithically integrated 900 V SSCBs realised in a scalable 4H-SiC JFET technology. With this novel concept, the effort of interrupting excessive DC current in case of failure is reduced from a whole system (e.g. sensor, µC, power switch, gate driver) to a single two pole device. Furthermore, the proposed plug-and-play SSCB stands out through ultra fast response time, while showing excellent avalanche capability. The scope of future developments focuses on scaling the trigger current level to several 10 A per chip to address the requirements of power electronic applications in DC grid and e-mobility environments.

»Thyristor Dual« Topology (Fig. 1a)

- Two complementary normally-on JFETs
- V_{DS} of one JFET is equal to V_{GS} of other JFET
- Intrinsic current controlled blocking mechanism

Monolithic Integration (Fig. 1b)

- 4H-SiC JFET technology revolves around re-epitaxy and SiC dry etching
- pJFET buried in the 1st epitaxial layer
- nJFET located in the 2nd epitaxial layer
- Floating source terminal (S) allows for observation of operating conditions

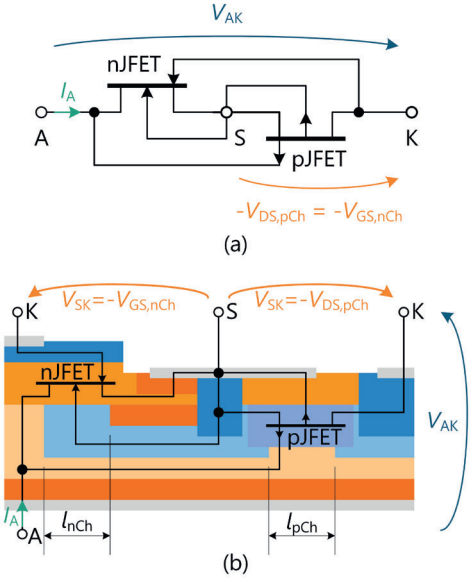


Fig. 1: Equivalent circuit diagram (a) and schematic cross section of the proposed monolithically integrated circuit breaker (b) [1, 2]

[1] N. Boettcher and T. Erlbacher, "A Monolithically Integrated SiC Circuit Breaker," IEEE Electron Device Letters, 2021.

[2] N. Boettcher and T. Erlbacher, "Fabrication Aspects and Switching Performance of a […] Circuit Breaker Device," ISPSD, 2022.

Analytical and Numerical Modelling (Fig. 2)

- Technology is extensively described in simulation models
- TCAD models allow for predictive cell design

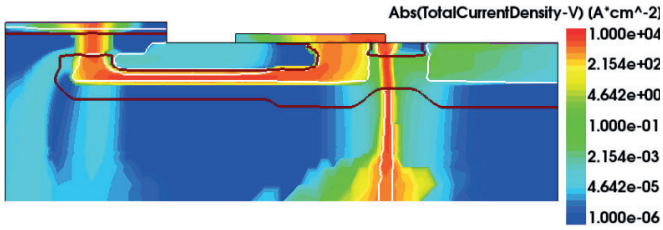


Fig. 2: TCAD simulation showing current flow under breakdown condition (reach-through) [3]

Scalable Output Characteristics (Fig. 3)

- Low resistive linear on-state region
  $R_{on,sp} \geq 650\ m\Omega cm^2$
- Self-sensed trigger mechanism
  $J_{trig} \leq 2.2\ Acm^{-2}$
- Self-sustained blocking state
  $V_{rt} \leq 900\ V$

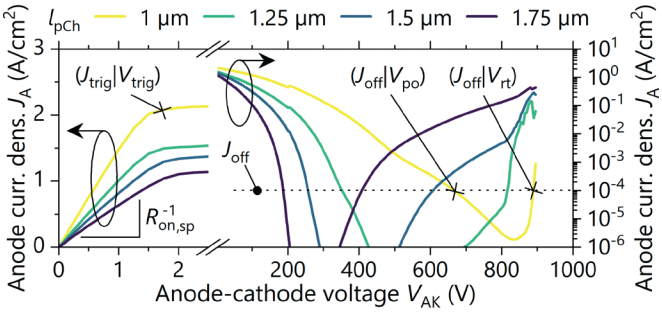
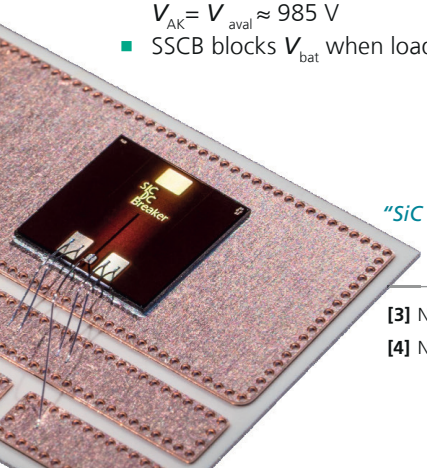


Fig. 3: Measured quasi-static output characteristics $J_A(V_{AK})$ for specific pJFET channel length values I_{pCh} [2]

Excellent Avalanche Capability during UIS (Fig. 4)

- Unclamped inductive switching (UIS) behaviour comparable to state-of-the-art power switches
- Intrinsic blocking mechanism triggered at
  $I_A = I_{trig} = 1.75\ A$
- SSCB conducts load current in avalanche state at
  $V_{AK} = V_{aval} \approx 985\ V$
- SSCB blocks V_{bat} when load current has fully subsided



"SiC DC-Breaker" chip on Cu substrate

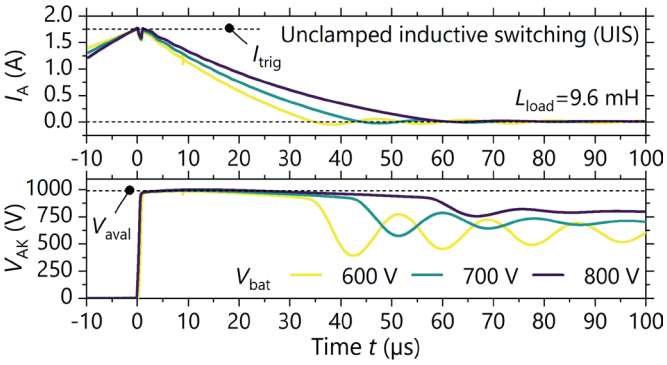


Fig. 4: Measured UIS response of anode current I_A and anode-cathode voltage V_{AK} for specific battery voltage values V_{bat} [2]

Ultra Fast Short Circuit Clearance (Fig. 5)

- Hard short circuit applied over the inductive load L_{load} at $I_A = 1\ A$ and $V_{bat} = 800\ V$
- SSCB blocks V_{bat} within ~100 ns
- 5-10 times faster than state-of-the-art SSCBs

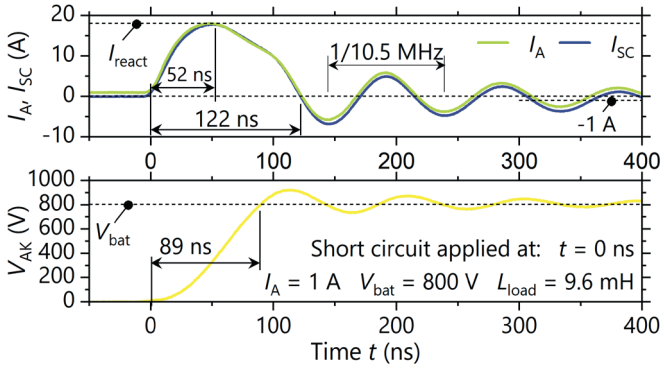


Fig. 5: Measured short circuit response of anode current I_A, short circuit current I_{SC} and anode-cathode voltage V_{AK} [4]

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[3] N. Boettcher and T. Erlbacher, "Design Considerations on a […] 900 V SiC Circuit Breaker," WiPDA Asia, 2020.

[4] N. Boettcher et al., "Short Circuit Performance and Current Limiting Mode of a […] SiC Circuit Breaker […]," EPE, 2022.